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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/744,522	01/25/2001	Peter Haas	P00,1963	8561

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EXAMINER	
MEINECKE DIAZ, SUSANNA M	
ART UNIT	PAPER NUMBER
3623	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/744,522	HAAS, PETER	
	Examiner	Art Unit	
	Susanna M. Diaz	3623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/25/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 have been cancelled by Applicant. Claims 10-20 have been added by preliminary amendment and are currently presented for examination.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because the amended specification is not on a separate sheet. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 10-14, 17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Khoyi et al. (U.S. Patent No. 5,634,124).

Khoyi discloses a system for data conversion, comprising:

[Claim 10] a processor having at least one unit for executing one of a logical or arithmetic operation and an object-oriented data conversion unit for recognizing a type of an object and an object address, the data conversion unit being arranged to precede the unit for executing a logical or arithmetic operation, whereby the data conversion unit recognizes said type of an object based upon a type of information accompanying the object address and matches the type of an object and the object address before one of an operation is performed or a predetermined type of object is generated in the event of non-match (Figs. 2, 4-8; col. 15, line 40 through col. 16, line 18; col. 23, lines 59-67; col. 34, lines 38-54; col. 36, lines 35-57; col. 38, lines 32-37 -- The various object tables specify links between parent and child objects, which implies existence of an address for each object in order to know where to access each respective object in memory. Each object also has a corresponding data type stored to indicate the object type. Object location indicators are stored in Fig. 6, # 366, as per col. 35, lines 46-51; col. 39, lines 1-15 -- Data conversion occurs when data types are different, i.e., when inequalities or non-matches have been identified; col. 15, line 40 through col. 16, line 39; col. 41, lines 2-23 -- Data conversion may take place at various stages of an operation, including prior to and/or after performance of an operation, prior to generation of a predetermined type of object, or prior to storage of the object in an external storage and a register file);

[Claim 11] wherein a memory location for the object address and a memory location of a register is respectively divided into a first area and a second area, whereby a type of the object is deposited in the first area (Figs. 2, 4-8; col. 15, line 40 through col. 16, line 18; col. 23, lines 59-67; col. 34, lines 38-54; col. 36, lines 35-57; col. 38, lines 32-37 -- The various object tables specify links between parent and child objects, which implies existence of an address for each object in order to know where to access each respective object in memory. Each object also has a corresponding data type stored to indicate the object type. Object location indicators are stored in Fig. 6, # 366, as per col. 35, lines 46-51);

[Claim 12] wherein the object-oriented data conversion unit is arranged to follow the unit executing a logical or an arithmetic operation (col. 15, line 40 through col. 16, line 39; col. 41, lines 2-23 -- Data conversion may take place at various stages of an operation, including prior to and/or after performance of an operation, prior to generation of a predetermined type of object, or prior to storage of the object in an external storage and a register file);

[Claim 13] wherein the object-oriented data conversion unit is arranged to precede the storing of the object in an external storage and a register file (col. 15, line 40 through col. 16, line 39; col. 41, lines 2-23 -- Data conversion may take place at various stages of an operation, including prior to and/or after performance of an operation, prior to generation of a predetermined type of object, or prior to storage of the object in an external storage and a register file);

[Claim 14] wherein a register file is divided into a memory area for data and a memory area for a respective type indication of the data (Figs. 2, 4-8; col. 15, line 40 through col. 16, line 18; col. 23, lines 59-67; col. 34, lines 38-54; col. 36, lines 35-57; col. 38, lines 32-37 -- The various object tables specify links between parent and child objects, which implies existence of an address for each object in order to know where to access each respective object in memory. Each object also has a corresponding data type stored to indicate the object type. Object location indicators are stored in Fig. 6, # 366, as per col. 35, lines 46-51).

Khoyi discloses a method for data conversion in a processor having at least one unit, the method comprising the steps of:

[Claim 17] executing a logical or arithmetic operation in the processor (Figs. 2, 4-8; col. 15, line 40 through col. 16, line 18; col. 23, lines 59-67; col. 34, lines 38-54; col. 36, lines 35-57; col. 38, lines 32-37);

implementing an object-oriented data conversion by a type information in an object address and by a type information of an object (Figs. 2, 4-8; col. 15, line 40 through col. 16, line 18; col. 23, lines 59-67; col. 34, lines 38-54; col. 36, lines 35-57; col. 38, lines 32-37); and

generating an inequality of the objects to be operated by the logical or arithmetic operation based upon the type of objects matched to one another or a predetermined object type of an object (Figs. 2, 4-8; col. 15, line 40 through col. 16, line 18; col. 23, lines 59-67; col. 34, lines 38-54; col. 36, lines 35-57; col. 38, lines 32-37 -- The various

object tables specify links between parent and child objects, which implies existence of an address for each object in order to know where to access each respective object in memory. Each object also has a corresponding data type stored to indicate the object type. Object location indicators are stored in Fig. 6, # 366, as per col. 35, lines 46-51; col. 39, lines 1-15 -- Data conversion occurs when data types are different, i.e., when inequalities or non-matches have been identified; col. 15, line 40 through col. 16, line 39; col. 41, lines 2-23 -- Data conversion may take place at various stages of an operation, including prior to and/or after performance of an operation, prior to generation of a predetermined type of object, or prior to storage of the object in an external storage and a register file);

[Claim 18] dividing a memory location for an object address and a memory location of a register into a first and second area of the object address (Figs. 2, 4-8; col. 15, line 40 through col. 16, line 18; col. 23, lines 59-67; col. 34, lines 38-54; col. 36, lines 35-57; col. 38, lines 32-37 -- The various object tables specify links between parent and child objects, which implies existence of an address for each object in order to know where to access each respective object in memory. Each object also has a corresponding data type stored to indicate the object type. Object location indicators are stored in Fig. 6, # 366, as per col. 35, lines 46-51); and

noting the data of the register deposited in the second area in the first area (Figs. 2, 4-8; col. 15, line 40 through col. 16, line 18; col. 23, lines 59-67; col. 34, lines 38-54; col. 36, lines 35-57; col. 38, lines 32-37 -- The various object tables specify links between parent and child objects, which implies existence of an address for each object

in order to know where to access each respective object in memory. Each object also has a corresponding data type stored to indicate the object type. Object location indicators are stored in Fig. 6, # 366, as per col. 35, lines 46-51).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 15, 16, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khoyi et al. (U.S. Patent No. 5,634,124), as applied to claims 10 and 17 above, in view of Microsoft Press® Computer Dictionary (Third Edition).

[Claims 15, 16, 19, 20] As per claims 15, 16, 19, and 20, Khoyi discloses a general operating system that utilizes a processor; however, Khoyi does not specify which type of processor is used. More specifically, Khoyi does not expressly teach the use of a reduced instruction set processor (RISC) or complex instruction set processor (CISC) as part of the disclosed invention. However, Microsoft Press® Computer Dictionary (Third Edition) defines both RISC and CISC as commonly utilized processors, each providing particular benefits over the other (pages 91, 412). For example, the definition of RISC clarifies that "RISC chips thus execute simple instructions more quickly than general-purpose CISC (complex instruction set computing) microprocessors, which are designed to handle a much wider array of instructions. They are, however, slower than

CISC chips at executing complex instructions, which must be broken down into many machine instructions that RISC microprocessors can perform." Since Khoyi must clearly operate utilizing one type of processor or another and RISC and CISC are both commonly utilized processors, the Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to implement Khoyi's invention using a reduced instruction set processor (as per claims 15 and 19) when more simple instructions are involved and need to be executed quickly or a complex instruction set processor (as per claims 16 and 20) when more complex instructions are involved and need to be executed quickly.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references disclose various systems/methods for performing data conversion:

Radia et al. (U.S. Patent No. 6,260,074)

Baisley (U.S. Patent No. 6,129,460)

Dyer et al. (U.S. Patent No. 5,754,849)

Cavendish et al. (U.S. Patent No. 5,276,816)

Koizumi et al. (US 2004/0154007)

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Susanna M. Diaz whose telephone number is (571) 272-6733. The examiner can normally be reached on Monday-Friday, 10 am - 6 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on (571) 272-6729. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Susanna Diaz
Susanna M. Diaz
Primary Examiner
Art Unit 3623

May 22, 2005